

## PATENT

IBM Docket No. RAL920000112US2

Amendments to the Claims:

- Sub  
B12  
A1
1. (Original) A system comprising:  
N different memories wherein  $N > 1$ ;  
M different busses with each one of the busses having a bandwidth to transport data at a predetermined rate, operatively coupled to one of the N memories wherein M is greater than 1;  
a plurality of memory controllers with each one of the plurality of memory controllers operatively coupled to one of the N memories, wherein said each one of the plurality of memory controllers setting an associated memory in a first mode or a second mode; and  
an arbiter responsive to at least one memory request signal to generate an Access vector that causes information to be read simultaneously from multiple ones of the N memory set in the first mode wherein total bandwidth on the busses of the multiple ones of the N memories is greater than the bandwidth on a single bus of one of the N memories.
  2. (Original) The system of Claim 1 wherein the first mode includes a Read mode.
  3. (Original) The system of claims 1 or 2 wherein each of the N memories includes DDR DRAM.
  4. (Original) The system of claim 3 wherein each of the DDR DRAM are partitioned into at least four banks and at least one buffer spread across the at least four banks.

Serial Number 09/990840

- 2 -

## PATENT

IBM Docket No. RAL920000112US2

- A1
5. (Original) The system of claim 4 wherein each buffer is partitioned into multiple maskable units.
  6. (Original) The system of claim 4 wherein each buffer is partitioned into four units.
  7. (Original) The system of claim 6 wherein each unit is equivalent to 1/4 the size of the buffer.
  8. (Original) The system of claim 6 wherein each unit is maskable.
  9. (Original) The system of claim 1 wherein the arbiter includes a controller executing a slice selection algorithm comprising the steps of:
    - Exclude slices scheduled for re-fresh cycle (indicated by each DRAM controller)
    - Assign slices for all R requests of Transmitter controller
    - Complement R-accesses from corresponding EPC queue [Slice; QW]
    - Assign slice to EPC for globally W excluded slices (e.g. slice is excluded by all slice exclusion rules from Receiver)
    - Assign slices to W requests in RR (Round Robin) fashion between non-excluded slices starting from last assigned slice (slice assigned to Receiver Controller in previous window)
    - Complement W-accesses by EPC accesses from corresponding EPC queue [Slice; QW] and
    - Assign slice to EPC requests according to priority expressed by Weight.

Serial Number 09/990840

- 3 -

**PATENT**  
**IBM Docket No. RAL920000112US2**

**10 - 22. (Canceled)**

- AI
- 23. (Original) A method comprising the acts of:**  
    **providing a plurality of separate memory elements in which frames**  
    **from communication device is to be stored or retrieved;**  
    **partitioning the frame with a controller into at least two parts;**  
    **storing each one of the at least two parts into different memory**  
    **elements if the at least two parts are adjoining parts of the same frame.**
- 24. (Original) The method of claim 23 further including the acts of an arbiter**  
    **in response to a request causing the memories to be read simultaneously**  
    **wherein each one of the two parts is available simultaneously on**  
    **respective busses associated with each one of the memory elements.**
- 25. (Original) A method including the acts of:**  
    **providing a plurality of separate memories in which data is stored;**  
    **receiving in an arbiter a request to read data from selected ones of**  
    **said plurality of separate memories; and**  
    **simultaneously reading said memories to provide data**  
    **simultaneously on individual busses coupled to the selected ones of said**  
    **plurality of separate memories.**
- 26. (Original) The method of claim 25 wherein the bandwidth of data on**  
    **each individual bus is less than the total bandwidth on activated busses.**

**Serial Number 09/990840**

**- 4 -**

**PATENT****IBM Docket No. RAL920000112US2**

- AI
27. (Original) A method comprising the acts of:
- providing a plurality of separate memory modules in which frames from communication devices can be stored;
  - partitioning a frame into multiple parts;
  - writing adjacent parts of the frame in different ones of the memory modules; and
  - simultaneously accessing multiple memory modules in a single memory access window to read data therefrom wherein the total bandwidth of data output from the multiple memory modules matches the bandwidth of a FAT pipe port on a communication device.
28. (Original) The system of claim 9 wherein the controller includes a state machine or other hardware circuits.
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